Docket No.: 1614.1393 Serial No. 10/796,005

IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claim 3 and AMEND claims 1 and 4 in accordance with the following:

1. (CURRENTLY AMENDED) A circuit for changing clocks, comprising:

a clock generating circuit ~~which generates~~ generating an output clock signal by controlling a frequency of an original clock signal~~;~~ and comprising:

a frequency divider which performs frequency division, and

a decimated clock generating circuit which decimates clock pulses; and

a control circuit ~~which controls~~ controlling said clock generating circuit in response to an operation mode change signal, indicative of a change from a first operation mode to a second operation mode of an external circuit operating based on the output clock signal, thereby changing the output clock signal from a first frequency corresponding to the first operation mode to a third frequency and then from the third frequency to a second frequency corresponding to the second operation mode, the third frequency having a frequency between the first frequency and the second frequency.

2. (ORIGINAL) The circuit as claimed in claim 1, wherein said control circuit controls said clock generating circuit so as to change the third frequency gradually between the first frequency and the second frequency.

3. (CANCELLED)

4. (CURRENTLY AMENDED) The circuit as claimed in claim 1, wherein~~: said clock generating circuit includes:~~

~~a~~ the frequency divider ~~which~~ generates one or more frequency-divided clock signals by dividing the original clock signal;

said clock generating circuit further comprises a selector circuit which selects one of the original clock signal and said one or more frequency-divided clock signals as a selected clock signal; ~~and~~

~~a~~ the decimated clock generating circuit ~~which~~ decimates one or more clock pulses of the selected clock signal for outputting as the output clock signal; and

~~wherein~~ said control circuit controls the selection performed by said selector circuit and the decimation performed by said decimated clock generating circuit in response to the operation mode change signal.

5. (ORIGINAL) The circuit as claimed in claim 4, wherein said control circuit includes a memory circuit for storing data indicative of a time duration in which the intervening frequency is maintained.

6. (ORIGINAL) The circuit as claimed in claim 5, wherein each said data stored in said memory circuit corresponds to one of a plurality of different types of the operation mode change signal.

7. (ORIGINAL) The circuit as claimed in claim 4, wherein said control circuit includes a register for storing a rate of the pulse decimation performed by said decimated clock generating circuit.

8. (ORIGINAL) The circuit as claimed in claim 7, wherein each said rate stored in said register corresponds to one of a plurality of different types of the operation mode change signal.

9. (ORIGINAL) The circuit as claimed in claim 1, wherein the operation mode change signal is one of a plurality of types of operation mode change signals, and said control circuit changes the controlling of said clock generating circuit depending on a type of the operation mode change signal.

10. (ORIGINAL) The circuit as claimed in claim 9, wherein the operation mode change signals include an operation mode change signal indicative of a change to a state in which an operation of the external circuit is suspended and an operation mode change signal indicative of a change to a state in which the operation of the external circuit is restored.